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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/663,911	ELLIS, FRAMPTON E.	
	Examiner	Art Unit	
	LASHANYA R. NASH	2453	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-25,27,28 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-25,27,28 and 30-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/6/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to the amendment filed 28 September 2009 and supplemental amendment filed 25 November 2009. Claims 1, 26, and 29 are cancelled. Claims 2-4, 8, 10-25, 27, 28, 30, and 31 are currently amended. Claims 32, 33 and 34 are new. Claims 2-25, 27, 28, and 30-34 are presented for further consideration.

Response to Arguments

Applicant's arguments (i.e. the internal firewall creates a protected portion of the microchip and an unprotected portion of the microchip which features are not shown in Force, G or Shaw), see Remarks, filed 25 November 2009, with respect to the rejections of claims 1-25 under 35 USC 103 have been fully considered and are persuasive in light of the amendments. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of a newly found prior art reference McKelvey (US Patent 5,896,499), as set forth below in the Office action.

Further consideration of dependent claims 2, 4,8,11-13,15-19,21-23, 27 and 30 are made, and a new grounds of rejection is made in view of a newly found prior art reference McKelvey (US Patent 5,896,499), as set forth below in the Office action.

Information Disclosure Statement

The information disclosure statement (IDS) submitted 6 January 2010 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2-4, 7-13, 19, 22-25, 27-34 are rejected under 35 U.S.C. 102(e) as being anticipated by McKelvey (US Patent 5,896,499), hereinafter referred to as McKelvey.

In reference to claim 32, McKelvey discloses:

- A personal computer configured for a connection to a network of computers including the Internet (i.e. computer system in communication with network systems; abstract), comprising:
- a microchip including (i.e. integrated circuit device; column 6, lines 45-57);
- a microprocessor, the microprocessor including (i.e. microprocessors of the central processing unit; column 6, lines 45-57);

- a master control unit (i.e. main processor) that is configured using hardware and firmware, and at least two processing units (i.e. multiple microprocessors of the main processor); the master control unit of the microprocessor being further configured to allow a user of the personal computer to control the processing units of the microprocessor (i.e. main processor controls operation of the computer system; column 6, lines 45-57) ;

- an internal hardware firewall (i.e. firewall capabilities of embedded security processor; column 7, lines 25-41) creating a protected portion of the microchip (i.e. main processor) and an unprotected portion of the microchip (i.e. security processor), (column 8, lines 11-25);

- said protected portion of the microchip including at least said master control unit of the microprocessor, and at least one of the processing units of the microprocessor (i.e. the main processor portion is protected from communication with the unsecure network; column 8, lines 25-35) ,

- said unprotected portion of the microchip including one or more of the processing units of the microprocessor (i.e. all communication accesses security processor; column 8, lines 20-25)

- said hardware firewall denying access to said protected portion of the microchip by a network including the Internet (i.e. security processor provides firewall security from the Internet; column 8, lines 11-16) when the personal

computer is connected to the network including the Internet (i.e. embedded security processor block all unwanted network traffic; column 8, lines 25-35) and

- said hardware firewall permitting access by another computer in the network including the Internet to said one or more of the processing units included in the unprotected portion of the microchip for an operation with said another computer in the network including the Internet when the personal computer is connected to the network including the Internet (i.e. all network communication passes through security processor; column 8, lines 16-25) and

- an active configuration of a circuit integrated into the microchip (i.e. column 6, lines 45-57).

In reference to claim 33, McKelvey discloses:

- A computer configured for a connection to a network of computers including the Internet (i.e. computer system in communication with network systems; abstract), comprising:

- a master controlling device (i.e. central processing unit) that is configured using hardware and firmware (column 6, lines 49-57), at least two microprocessors (i.e. microprocessors of central processing unit; column 6, lines 49-57); and

- the master controlling device of the computer being further configured to allow a user of the personal computer to control the microprocessors (column 6, lines 45-57);

- an internal hardware firewall (i.e. firewall capabilities of embedded security processor; column 7, lines 25-41) creating a protected portion of the computer (i.e. main processor) and an unprotected portion (i.e. security processor) of the computer (column 8, lines 11-25);

- said protected portion of the computer including at least said master controlling device, and at least one of the microprocessors (i.e. the main processor portion is protected from communication with the unsecure network; column 8, lines 25-35) ,

- said unprotected portion of the computer including one or more of the microprocessors (i.e. all communication accesses security processor; column 8, lines 20-25);

- said hardware firewall denying access to said protected portion of the computer by a network including the Internet (i.e. security processor provides firewall security from the Internet; column 8, lines 11-16) when computer is connected to the network including the Internet (i.e. embedded security processor block all unwanted network traffic; column 8, lines 25-35); and

- said hardware firewall permitting access by another computer in the network including the Internet to said one or more of the microprocessors included in the unprotected portion of the computer for an operation with said another computer in the network including the Internet when the personal computer is connected to the network including the Internet (i.e. all network communication passes through security processor; column 8, lines 16-25); and

- an active configuration of motherboard hardware (i.e. column 6, lines 45-57).

In reference to claim 34, McKelvey discloses:

- A microchip (i.e. integrated circuit device; column 6, lines 45-57) configured for a connection to a network of computers including
  the Internet (abstract), comprising:

- a microprocessor, the microprocessor including a master control unit that is configured using hardware and firmware, and at least two processing units (i.e. main processor; column 6, lines 45-57);

- the master control unit of the microprocessor being further configured to allow a user of the personal computer to control the processing units of the microprocessor (column 6, lines 45-57);

- an internal hardware firewall (i.e. firewall capabilities of embedded security processor; column 7, lines 25-41) creating a protected portion (i.e. main processor) of the microchip and an unprotected portion (i.e. security processor) of the microchip (column 8, lines 11-25); ;

- said protected portion of the microchip including at least said master control unit of the microprocessor, and at least one of the processing units of the microprocessor (i.e. the main processor portion is protected from communication with the unsecure network; column 8, lines 25-35) ,

- said unprotected portion of the microchip including one or more of the processing units of the microprocessor (i.e. all communication accesses security processor; column 8, lines 20-25);

- said hardware firewall denying access to said protected portion of the microchip by a network including the Internet (i.e. security processor provides firewall security from the Internet; column 8, lines 11-16) when the personal computer is connected to the network including the Internet (i.e. embedded security processor block all unwanted network traffic; column 8, lines 25-35); and

- said hardware firewall permitting access by another computer in the network including the Internet to said one or more of the processing units included in the unprotected portion of the microchip for an operation with said another computer in the network including the Internet when the personal computer is connected to

the network including the Internet (i.e. all network communication passes through security processor; column 8, lines 16-25); and

- an active configuration of a circuit integrated into the microchip 9(i.e. column 6, lines 45-57).

In reference to claims 2, 27, and 30 McKelvey discloses the personal computer of claim 32, wherein the said protected portion of the microchip includes a non-volatile memory (i.e. main memory; column 6, lines 58-64).

In reference to claim 3, McKelvey discloses the personal computer of claim 2, wherein the internal hardware firewall is also-configured using firmware (column 8, lines 36-38).

In reference to claim 4, McKelvey discloses the personal computer of claim 2, wherein said unprotected portion of the microchip includes volatile memory (column 7, lines 51-59).

In reference to claim 7, McKelvey discloses the personal computer of claim 2, wherein the active configuration is used to configure said firewall (column 8, lines 36-54).

In reference to claim 8, McKelvey discloses the personal computer of claim 2, wherein the master control unit is configured to control access to the unprotected portion of the microchip by the network including the Internet for said operation when the computer is connected to the network including the Internet (column 8, lines 17-25).

In reference to claim 9, McKelvey discloses the personal computer of claim 2, wherein the personal computer includes one or more of a telephone, a radio, a pager, a handheld personal digital assistant, a wearable computer, a digital signal processor, an entertainment device, a game, a videocam, an optical data recording device, a camera, a household electronic device, a business electronic device, and an automobile (column 5, lines 35-37).

In reference to claim 10, McKelvey discloses the personal computer of claim 2, wherein the network connection includes a direct wireless connection to the another computer (column 5, line 60-column 6, line 4).

In reference to claim 11, McKelvey discloses the personal computer of claim 2, wherein said unprotected portion of the microchip includes a non-volatile memory (column 7, lines 51-59).

In reference to claim 12, McKelvey discloses the personal computer of claim 2, wherein said unprotected portion of the microchip further includes a network communications component (column 7, line 60-column 8, line 10).

In reference to claim 13, McKelvey discloses the personal computer of claim 2, wherein said protected portion of the microchip further includes a flash memory component (column 6, lines 58-64).

In reference to claim 19, McKelvey discloses the personal computer of claim 2 wherein said unprotected portion of the microchip further includes a modem component of the personal computer (column 1, lines 40-47).

In reference to claim 22, McKelvey discloses the personal computer of claim 2 wherein the protected portion of the microchip is temporarily inaccessible from the network when the computer is connected to the network (column 8, lines 25-35).

In reference to claim 23, McKelvey discloses the personal computer of claim 2 wherein the protected portion of the microchip is permanently inaccessible from the network when the computer is connected to the network (column 8, lines 25-35).

In reference to claim 24, McKelvey discloses the personal computer of claim 2, wherein the internal hardware firewall has default settings that protect the personal computer from access from the Internet, but with the capability for a user of the personal computer to override the default settings (column 8, lines 36-55).

In reference to claims 25, 28, and 31 McKelvey discloses the personal computer of claim 2, wherein the configuration of the internal hardware firewall is controlled by a network administrator in a local network (column 11, lines 30-45).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 6 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKelvey as applied to claim 32 above and further in view of Romig et al., ("High Performance Microsystem Packaging: A Perspective"- retrieved from ScienceDirect database), hereinafter referred to as Romig.

In reference to claims 5 and 20, McKelvey fails to disclose the personal computer wherein the configuration is provided by the use of field-programmable gate arrays (FPGA's). Nonetheless, this was a well known feature at the time of the invention, as

further evidenced by Romig and thus would have been an obvious modification for one of ordinary skill in the art to the personal computer as disclosed by McKelvey.

In an analogous art, Romig discloses integrated Microsystems implemented onto microchips (*Abstract*; page 1771). Romig further discloses wherein the configuration is provided by the use of field-programmable gate arrays (FPGA's), (page 1777, paragraph 6). One of ordinary skill in the art would have been so motivated to accordingly modify the teachings of McKelvey so as to implement discrete devices (i.e. chip) with increased functionality, improved reliability and decreased costs (*Introduction*; page 1771).

In reference to claim 6, McKelvey fails to disclose the personal computer wherein the configuration is provided by the use of micro-electromechanical systems (MEMS). Nonetheless, this was a well known feature at the time of the invention, as further evidenced by Romig and thus would have been an obvious modification for one of ordinary skill in the art to the personal computer as disclosed by McKelvey.

In an analogous art, Romig discloses integrated Microsystems implemented onto microchips (abstract; page 1771). Romig further discloses wherein the configuration is provided by the use of micro-electromechanical systems (MEMS), (*Introduction*; page 1771). One of ordinary skill in the art would have been so motivated to accordingly modify the teachings of McKelvey so as to implement discrete devices (i.e. chip) with increased functionality, improved reliability and decreased costs (introduction; page 1771).

Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKelvey as applied to claim 32 above and further in view of Shaw et al. (US Patent 5,754,766) hereinafter referred to as Shaw and McKelvey respectively.

In considering 14, McKelvey fails to disclose the personal computer wherein the flash memory component includes a BIOS (basic input/output system) of the personal computer. Nonetheless, this was a well known feature at the time of the invention, as further evidenced by Shaw and thus would have been an obvious modification for one of ordinary skill in the art to the personal computer as disclosed by McKelvey.

In an analogous art, Shaw discloses an integrated circuit system (abstract). Shaw further discloses a computer where the flash memory component includes a BIOS (basic input/output system) of the personal computer (column 33, lines 45-52). One of ordinary skill in the art would have motivated to accordingly modify the teachings of Mckelvey so as to provide an integrated circuit with optimum computational performance (Shaw; abstract).

In considering 15, McKelvey fails to disclose the personal computer wherein the unprotected portion of the microchip includes a sound component of the personal computer. Nonetheless, this was a well known feature at the time of the invention, as further evidenced by Shaw and thus would have been an obvious modification for one of ordinary skill in the art to the personal computer as disclosed by McKelvey.

In an analogous art, Shaw discloses an integrated circuit system (abstract). Shaw further discloses a computer wherein the microchip includes a sound component of the personal computer (column 32, lines 40-52). One of ordinary skill in the art would have motivated to accordingly modify the teachings of Mckelvey so as to provide an integrated circuit with optimum computational performance (Shaw; abstract).

In considering 16, McKelvey fails to disclose the personal computer wherein the unprotected portion of the microchip includes a graphics component of the personal computer. Nonetheless, this was a well known feature at the time of the invention, as further evidenced by Shaw and thus would have been an obvious modification for one of ordinary skill in the art to the personal computer as disclosed by McKelvey.

In an analogous art, Shaw discloses an integrated circuit system (abstract). Shaw further discloses a computer wherein the microchip includes a graphics component of the personal computer (column 6, lines 40-46; column 32, lines 40-52). One of ordinary skill in the art would have motivated to accordingly modify the teachings of Mckelvey so as to provide an integrated circuit with optimum computational performance (Shaw; abstract).

In considering 17, McKelvey fails to disclose the personal computer wherein the unprotected portion of the microchip includes a video processing component of the personal computer. Nonetheless, this was a well known feature at the time of the

invention, as further evidenced by Shaw and thus would have been an obvious modification for one of ordinary skill in the art to the personal computer as disclosed by McKelvey.

In an analogous art, Shaw discloses an integrated circuit system (abstract). Shaw further discloses a computer personal computer wherein the microchip includes a video processing component of the personal computer (column 6, lines 40-46; column 32, lines 40-52). One of ordinary skill in the art would have motivated to accordingly modify the teachings of Mckelvey so as to provide an integrated circuit with optimum computational performance (Shaw; abstract).

In considering 18, McKelvey fails to disclose the personal computer wherein the unprotected portion of the microchip includes an analog component of the personal computer. Nonetheless, this was a well known feature at the time of the invention, as further evidenced by Shaw and thus would have been an obvious modification for one of ordinary skill in the art to the personal computer as disclosed by McKelvey.

In an analogous art, Shaw discloses an integrated circuit system (abstract). Shaw further discloses a computer personal computer wherein the microchip includes an analog component of the personal computer (column 6, lines 63-67). One of ordinary skill in the art would have motivated to accordingly modify the teachings of Mckelvey so as to provide an integrated circuit with optimum computational performance (Shaw; abstract).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over McKelvey as applied to claim 32 above and further in view of Chin et al. (US Patent 5,497,465), hereinafter referred to as Chin.

In reference to claim 21 McKelvey fails to disclose the personal computer of claim 2, wherein the unprotected portion of the microchip includes at least four or eight or 16 or 64 or 128 or 256 or 512 or 1024 of said processing units of the microprocessor. Nonetheless, this would have been an obvious modification to the personal computer of Shaw and Force for one of ordinary skill in the art at the time of the invention, as further evidenced by Chin.

In an analogous art, Chin discloses a parallel processing system which employs a processing chip (abstract). Chin further discloses wherein the microchip includes at least four or eight or 16 or 64 or 128 or 256 or 512 or 1024 of said processing units of the microprocessor (i.e. 64 processors), (column 10, lines 30-46). One of ordinary skill in the art would have been so motivated to accordingly modify the personal computer of McKelvey so as to improve operation speed and accuracy for higher speed computing (Chin; column 3, lines 45-54).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LASHANYA R. NASH whose telephone number is (571)272-3957. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Thomas can be reached on (571) 272-6776. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/THUHA T. NGUYEN/
Primary Examiner, Art Unit 2453

/LaShanya R Nash/
Examiner, Art Unit 2453
February 24, 2010